

## In the Claims

1. A method of forming a plurality of DRAM capacitors comprising:  
etching capacitor container openings for an array in a substrate in at  
least two separate etching steps, and forming electrically insulative partitions  
between adjacent capacitors intermediate the two etching steps.

2. The method of claim 1, wherein the forming electrically insulative  
partitions step comprises:

forming insulative material over the substrate; and  
conducting an anisotropic etch of the insulative material to a degree  
sufficient to leave the partitions.

Claim 53 was previously canceled.

3. The method of claim 1, wherein forming electrically insulative  
partitions comprises depositing a dielectric layer.

4. The method of claim 1, wherein etching capacitor container  
openings comprises:

anisotropically etching first capacitor container openings in a first  
etching step; and

anisotropically etching second capacitor container openings in a second  
etching step.

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56. The method of claim 51, wherein etching capacitor container openings comprises:

anisotropically etching first capacitor container openings; and  
anisotropically etching second capacitor container openings.

57. (Amended) A method of forming a plurality of DRAM capacitors comprising:

anisotropically etching first capacitor container openings; and  
subsequently anisotropically etching second capacitor container openings, the first and second capacitor container openings being formed on a common substrate.

58. The method of claim 57, wherein the second capacitor container openings are intercalated between the first capacitor container openings.

59. The method of claim 57, wherein the second capacitor container openings are intercalated between the first capacitor container openings, the method further comprising forming electrically insulative partitions between adjacent capacitors intermediate etching the first and second capacitor container openings.



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CONT*

9. A method of forming a plurality of DRAM capacitors comprising:  
anisotropically etching first capacitor container openings in a first dielectric layer;

forming electrically insulative partitions between adjacent capacitors after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer after forming electrically insulative partitions.

10. A method of forming a plurality of DRAM capacitors comprising:  
anisotropically etching first capacitor container openings in a first dielectric layer;

forming a second dielectric layer over the substrate, the second dielectric layer comprising a different material than the first dielectric layer;

conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave partitions, after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first dielectric layer.



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62. A method of forming a plurality of DRAM capacitors comprising:  
anisotropically etching first capacitor container openings in a first  
dielectric layer;

forming electrically insulative partitions between adjacent capacitors  
after anisotropically etching first capacitor container openings; and

anisotropically etching second capacitor container openings in the first  
dielectric layer after forming electrically insulative partitions.

63. The method of claim 62, wherein forming electrically insulative  
partitions comprises:

depositing a second dielectric layer; and  
conducting an anisotropic etch of the second dielectric layer to a degree  
sufficient to leave the partitions.

64. The method of claim 62, wherein the first dielectric layer  
comprises silicon dioxide.

65. The method of claim 62, wherein the first dielectric layer  
comprises borophosphosilicate glass.

~~15.~~ 66. A method of forming a plurality of DRAM capacitors comprising:  
anisotropically etching first capacitor container openings in a first  
dielectric layer;

forming electrically insulative partitions between adjacent capacitors  
after etching the first capacitor container openings; and

anisotropically etching second capacitor container openings in the first  
dielectric layer after forming electrically insulative partitions, the first and  
second capacitor container openings being formed on a common substrate.

~~16.~~ 67. The method of claim ~~66~~ 15, wherein the second capacitor container  
openings are intercalated between the first capacitor container openings.

~~17.~~ 68. The method of claim ~~66~~ 15, wherein the second capacitor container  
openings are intercalated between the first capacitor container openings,  
wherein forming electrically insulative partitions comprises:

depositing a second dielectric layer; and  
conducting an anisotropic etch of the second dielectric layer to a degree  
sufficient to leave the partitions.

*D1*  
Cont

*H* 69 15 The method of claim 69, wherein forming electrically insulative partitions comprises:

depositing a second dielectric layer; and  
conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave the partitions.

**New Claims**

*D2* 10. A method of forming a plurality of DRAM capacitors comprising:  
anisotropically etching first capacitor container openings in a first dielectric layer in a first etching step;  
forming a second dielectric layer over the substrate and the first capacitor container openings;  
conducting an anisotropic etch of the second dielectric layer to a degree sufficient to leave electrically insulative sidewall spacers on sidewalls of the first capacitor container openings;  
after etching the second dielectric layer, anisotropically etching second capacitor container openings in the first dielectric layer in a second etching step, the second etching step etching the first dielectric layer selectively with respect to the second dielectric layer, the second capacitor containers being intercalated between the first capacitor container openings, at least one of the first capacitor container openings being spaced from at least one second capacitor container opening by a distance no greater than a width of an interposed electrically insulative sidewall spacer.



*20* The method of claim *19* wherein the first dielectric layer comprises silicon dioxide.

*21* The method of claim *19* wherein the first dielectric layer comprises borophosphosilicate glass.

